52. The integrated circuit of claim 51, further comprising:

a transposer coupled to the memory and selectively configured to transpose the outbound data when the integrated circuit function is an input layer chip and to transpose the inbound data when the integrated circuit function is an output layer chip.

53. The integrated circuit of claim 52, further comprising:

a sorter coupled to the memory and selectively configured to sort the inbound data when the integrated circuit function is an input layer chip and to sort the inbound data when the integrated circuit function is an intermediate layer chip.

54. The integrated circuit of claim 51, wherein:

the memory is a buffer memory that includes a plurality of queues;

when the integrated circuit function is an input layer chip, the memory includes N queues corresponding to N output terminals;

when the integrated circuit function is an intermediate layer chip, the memory includes N buffers positioned between N input terminals and N output terminals; and

when the integrated circuit function is an output layer chip, the memory includes an N-deep queue corresponding to N input terminals.

55. The network switch of claim 54, wherein the input layer chip includes:

a sorting circuit to route incoming cells to one of N destinations, each destination of the N destinations having a corresponding queue within the input layer circuit; and

a transposer circuit coupled to the N queues and the N output terminals, the transposer circuit being configured to transpose cells stored in the N queues for delivery to the N output terminals.

56. The network switch of claim 54, wherein the intermediate layer chip includes:

a sorting circuit to route incoming cells to the N buffers, the N buffers thereafter delivering the incoming cells to the N intermediate layer circuit output terminals.

57. The network switch of claim 54, wherein the output layer chip includes:

a transposer circuit coupled to the N output layer circuit input terminals, the transposer circuit being configured to transpose data cells received at the N output layer circuit input terminals; and

an output layer circuit queue coupled to the transposer circuit and the output layer circuit output port.

58. An integrated circuit, comprising:

an input port for receiving inbound data from one or more input terminals;

an output port for transmitting outbound data to one or more output terminals;

a memory coupled to the input port and configured to store inbound data received at the input port;

a module logic circuit coupled to the memory, the module logic circuit being enabled to implement a single circuit selected from an input layer circuit, an intermediate layer circuit and an output layer circuit; and

a scheduler coupled to the module logic circuit, the scheduler being configured to selectively store data in the memory based at least in part on the selected single circuit.

59. The integrated circuit of claim 58, further comprising:

a transposer coupled to the memory and selectively configured to transpose the outbound data when the selected single circuit is an input layer circuit and to transpose the inbound data when the selected single circuit is an output layer circuit.

60. The integrated circuit of claim 58, further comprising:

a sorter coupled to the memory and selectively configured to sort the inbound data when the selected single circuit is an input layer circuit and to sort the inbound data when the selected single circuit is an intermediate layer circuit.

61. The integrated circuit of claim 58, wherein:

the memory is a buffer memory that includes a plurality of queues;

when the selected single circuit is an input layer circuit, the memory includes N queues corresponding to N output terminals;

when the selected single circuit is an intermediate layer circuit, the memory includes N buffers positioned between N input terminals and N output terminals; and

when the selected single circuit is an output layer circuit, the memory includes an N-deep queue corresponding to N input terminals.

62. The network switch of claim 61, wherein the input layer circuit includes:

a sorting circuit to route incoming cells to one of N destinations, each destination of the N destinations having a corresponding queue within the input layer circuit; and

a transposer circuit coupled to the N queues and the N output terminals, the transposer circuit being configured to transpose cells stored in the N queues for delivery to the N output terminals.

63. The network switch of claim 61, wherein the intermediate layer circuit includes:

a sorting circuit to route incoming cells to the N buffers, the N buffers thereafter delivering the incoming cells to the N intermediate layer circuit output terminals.

64. The network switch of claim 61, wherein the output layer circuit includes:

a transposer circuit coupled to the N output layer circuit input terminals, the transposer circuit being configured to transpose data cells received at the N output layer circuit input terminals; and

an output layer circuit queue coupled to the transposer circuit and the output layer circuit output port.